CLAIMS

The invention is limited only as defined in the following claims and equivalents thereof.

We claim:

1. A device to measure gate critical dimension (CD) in different positions on a semiconductor wafer, said device comprising:

   an oxide layer or similar insulating layer deposed on a silicon wafer;

   a polysilicon layer, or a layer of any other material or set of steps and materials as used or similar to those used to manufacture transistor gates, henceforth referred to as the "gate" layer, deposed on the oxide or insulating layer, patterned to form resistors and other shapes; and

   a grid, where each site contains copies of several resistors, each with surrounding shapes composed of the same materials as the resistors.

2. The device in claim 1, wherein said resistors and surrounding features correspond to gates that are likely to be found in an integrated circuit (IC) layout, as defined by the physical design rules; wherein each resistor has specific features, such as, but not limited to:

   a specified orientation (for example, but not limited to vertical, horizontal, 45 degree orientations); and

   a neighborhood of other features composed of the same material and created with the same fabrication steps (for example, but not limited to nearby features with a specified distance to the resistor, possibly differentiating between features to the north, south, east, and west of the resistor).

3. A method for labeling all gates in a specific integrated circuit (IC) layout, according to any or all of the features below:

   A. classifying all gates in the said layout of a circuit depending on orientation (for example, but not limited to vertical, horizontal, 45 degrees orientations);

B. classifying all gates in a circuit design with a physical layout depending on their neighborhood, i.e. set of nearby features in the same layer of the layout (for example, but not limited to distance to nearest neighbors and more distant neighbors and/or a complete description of the neighborhood, as defined by a physical distance to other features); and

C. classifying all gates in a circuit design within a physical layout depending on the relative positions of neighboring structures in the same layer of the layout (for example, east vs. west neighbors, north vs. south neighbors, and/or a complete description of the neighborhood, as defined by physical distance and location of adjacent structures with respect to each said gate).

4. A method for determining the most frequent gate categories in a specific integrated circuit (IC) layout, said method including steps of:

A. labeling all gates according to the method of claim 3;

B. determining the number of gates in each category in step A; and

C. selecting the categories with the largest number of gates.

5. A device to measure gate critical dimension (CD) in different positions on the semiconductor wafer, said device comprising:

an oxide or similar insulating layer deposed on a silicon wafer;

a polysilicon layer, or a layer of any other material or set of steps and materials as used or similar to those used to manufacture transistor gates, referred to as the "gate" layer, deposed on the oxide or insulating layer, patterned to form resistors and other shapes, wherein said resistors and surrounding features are selected to correspond to the most frequent features in a specific integrated circuit (IC) layout, according to the method of claim 4; and

a grid, where each site contains copies of several resistors, each with surrounding shapes composed of the same materials as the resistors.

6. The device in claim 1, 2, or 5, said device further comprising a detector containing four pads, composed of polysilicon and/or other materials, as needed to connect to

each resistor, two on each end, to be measured by attaching (a) a current generator for applying a current through each resistor and (b) a voltage meter for measuring the voltage across each of the resistors and wherein the measured voltage is used to calculate the resistance and width (CD) of each resistor.

7. A device to measure gate critical dimension (CD) in different positions on the semiconductor wafer, said device comprising:

transistors and other shapes, wherein said transistors and surrounding features correspond to gates that are likely to be found in an integrated circuit (IC) layout, as defined by the physical design rules; wherein each transistor has specific features, such as, but not limited to (a) a specified orientation (for example, but not limited to vertical, horizontal, 45 degree orientations) and (b) a neighborhood of other features composed of the same gate materials (for example, but not limited to nearby features with a specified distance to the transistor, possibly differentiating between features to the north, south, east, and west of the transistor); and

a grid, where each site contains copies of several transistors, each with surrounding shapes.

8. A device to measure gate critical dimension (CD) in different positions on the semiconductor wafer, said device comprising:

transistors and other shapes, wherein said transistors and surrounding features correspond to gates that are likely to be found in an integrated circuit (IC) layout, as defined by the physical design rules; wherein said transistors and surrounding features are selected to correspond to the most frequent features in a specific integrated circuit (IC) layout, according to the method of claim 4; and

a grid, where each site contains copies of several transistors, each with surrounding shapes.

9. A method for representing the gate critical dimension (CD) within an optical field on a semiconductor wafer, said method including the steps of:

A. fabricating a collection of semiconductor wafers including multiple copies of the device of claim 6, according to the lithographic and manufacturing procedures as used for printing the "gate" layer and other relevant steps of other integrated circuits;

B. measuring the device by (a) attaching a current generator for applying a current through each resistor and (b) attaching a voltage meter for measuring the voltage across each of the resistors, to find the CD for each resistor, where each resistor is labeled according to position within the optical field (x,y), category (cat), and instance (i), to produce a data set with values CD(x,y,cat,i); and

C. representing the gate critical dimension within a optical field as CD(x,y,cat) by averaging values for each instance.

10. A method for representing the gate critical dimension (CD) within a optical field on a semiconductor wafer, said method including the steps of:

A. fabricating a collection of semiconductor wafers including multiple copies of the device of claim 6, according to manufacturing procedures used for other integrated circuits, except varying the lithographic procedures for printing the "gate" layer (focus, exposure settings, for example) to include conditions representing manufacturing extremes according to an experimental design, as would be understood by those skilled in the art;

B. measuring the device by (a) attaching a current generator for applying a current through each resistor and (b) attaching a voltage meter for measuring the voltage across each of the resistors, to find the CD for each resistor, where each resistor is labeled according to position within the optical field (x,y), category (cat), and instance (i), to produce a dataset with values CD(x,y,cat,i); and

C. representing the gate critical dimension within the optical field as CD(x,y,cat) by averaging the values for each instance, or by applying a weighted averaging technique.

11. A method for representing the gate critical dimension (CD) within an optical field on a semiconductor wafer, said method including the steps of:

A. fabricating a collection of semiconductor wafers including multiple copies of the device of claim 1, 2, 5, 7, or 8, according to the lithographic and manufacturing procedures as used for printing the "gate" layer and other relevant steps of other integrated circuits, until completion of patterning of the "gate" layer;

B. measuring the CD of each instance of each gate or resistor with standard methods apparent to those of ordinary skill in the art (i.e. optical techniques) where each measurement is labeled according to the position within the optical field (x,y), category (cat), and instance (i), to produce a data set with values CD(x,y,cat,i); and

C. representing the gate critical dimension within the optical field by averaging the values for each instance.

12. A method for representing the gate critical dimension (CD) within an optical field on a semiconductor wafer, said method including the steps of:

A. fabricating a collection of semiconductor wafers including copies of the device of claim 1, 2, 5, 7, or 8, according to manufacturing procedures used for other integrated circuits, until completion of patterning of the "gate" layer, except varying the lithographic procedures for printing the "gate" layer (focus, exposure settings, for example) to include conditions representing manufacturing extremes according to an experimental design, as would be understood by those skilled in the art;

B. measuring the CD of each instance of each gate or resistor with standard methods apparent to those of ordinary skill in the art (i.e. optical techniques), where each measurement is labeled according to the position within the optical field (x,y), category (cat), and instance (i), to produce a data set with values CD(x,y,cat,i); and

C. representing the gate critical dimension within the optical field as CD(x,y,cat) by averaging the values for each instance, or by applying a weighted averaging procedure.

13. A method for representing the gate critical dimension (CD) within a optical field on a semiconductor wafer used for fabrication of an integrated circuit, said method including the steps of:

A. fabricating a collection of semiconductor wafers using the standard procedures used for producing multiple copies of an integrated circuit product, until completion of patterning of the "gate" layer;

B. partitioning the optical field into segments, labeled by position (x,y), and identifying representative gates corresponding to each category (cat);

C. measuring the CD of each instance of each representative gate with standard methods apparent to those of ordinary skill in the art (i.e. optical techniques), where each measurement is labeled according to position within the optical field (x,y), category (cat), and instance (i), to produce a dataset with values CD(x,y,cat,i); and

D. representing the gate critical dimension within the optical field as CD(x,y,cat) by averaging the values for each instance.

14. A method for representing the gate critical dimension (CD) within a optical field on a semiconductor wafer used for fabrication of an integrated circuit, said method including the steps of:

A. fabricating a collection of semiconductor wafers using the standard procedures used for producing multiple copies of an integrated circuit product, until completion of patterning of the "gate" layer, except varying the lithographic procedures for printing the "gate" layer (focus, exposure settings, for example) to include conditions representing manufacturing extremes according to an experimental design, as would be understood by those skilled in the art;

B. partitioning the optical field into segments, labeled by position (x,y), and identifying representative gates corresponding to each category (cat);

C. measuring the CD of each instance of each representative gate with standard methods apparent to those of ordinary skill in the art (i.e. optical techniques), where each measurement is labeled according to position within the optical field

(x,y), category (cat), and instance (i), to produce a dataset with values CD(x,y,cat,i); and

D. representing the gate critical dimension within the optical field as CD(x,y,cat) by averaging the values for each instance, or by applying a weighted averaging procedure.

15. The method of claim 9, 10, 11, 12, 13, or 14, further including steps of:

A. calibrating (optimizing internal settings of) a lithography or process simulator to best approximate measured data, CD(x,y,cat); and

B. using the same settings to run the lithography or process simulator to obtain CD(x,y,cat) for categories not included in the original data set.

16. The method of claim 10, 12, or 14, further including steps of:

A. averaging the values of CD(x,y,cat,i) for each different setting of the lithographic equipment (focus, exposure, for example), to obtain CD(x,y,cat,setting);

B. calibrating a lithography or process simulator to best approximate measured data, CD(x,y,cat,setting);

C. using the same settings to run the lithography or process simulator to obtain CD(x,y,cat,setting) for categories not included in the original data set; and

D. calculating CD(x,y,cat) for categories not included in the original data set by averaging CD(x,y,cat,setting), or by using a weighted averaging procedure.

17. A method for estimating circuit properties (power, speed, yield, etc.), said method including the steps of:

A. labeling all gates of a layout of the circuit by classifying gates by any or all of the following criteria to specify their category (cat): (i) orientation, (ii) neighborhood features within the same layer of the layout (for example, but not limited to the distance to nearest neighbors and/or more distant neighbors), and (iii) relative positions of neighboring structures within the same layer of the layout (for example, but not limited to east vs. west neighbors, north vs. south neighbors) and labeling all gates according to location in the optical field (x,y);

B. labeling the corresponding gates in the netlist according to category (cat) and location in the optical field (x,y);

C. finding the relation between gate length, L, in the netlist, and CD, as would be easily determined by one skilled in the art;

D. modifying the netlist by modifying L(x,y,cat) for each gate based on CD data, CD(x,y,cat), given any choice of CD(x,y,cat), determined by a method apparent to one of ordinary skill in the art or by any of the methods of claims 9, 10, 11, 12, 13, 14, 15, and 16, and where missing values of CD(x,y,cat) are determined via an interpolation procedure; and

E. inputting the modified netlist to standard software tools to estimate circuit properties (power, speed, yield, etc.).

18. A method for estimating properties (power, speed, yield, etc.) of each cell in a cell library and for creating a corresponding model of each cell, as a function of position (x,y) in the optical field, said method including the steps of:

A. determining CD(x,y,cat) by a method apparent to one of ordinary skill in the art or by any of the methods of claims 9, 10, 11, 12, 13, 14, 15, and 16;

B. determining the maximum and minimum values of CD(x,y,cat), for all values of x and y and all categories, and partitioning the range from the minimum to maximum values into segments;

C. determining the corresponding sets of values, x and y, corresponding to each segment for each category;

D. finding each set of values of x and y, with CD(x,y,cat) falling in the same segment for all categories, S(x,y);

E. labeling all gates of a layout of the cell in the cell library by any or all of the following criteria to specify their category (cat): (i) orientation, (ii) neighborhood features within the same layer of the layout (for example, but not limited to the distance to nearest neighbors and/or more distant neighbors), and (iii) relative positions of neighboring structures within the same layer of the layout (for example, but not limited to east vs. west neighbors, north vs. south neighbors) and

labeling the corresponding gates in the netlist according to category (cat), while assuming neighboring cells which have assumed features at an assumed distance;

F. finding the relation between gate length, L, in the netlist, and CD, as would be easily determined by one skilled in the art;

G. modifying the netlist corresponding to a cell in location S(x,y) by modifying L(cat) for each gate based on CD data, CD(x,y,cat), where missing values of CD(x,y,cat) are determined via an interpolation procedure; and

H. inputting the modified netlist to standard software tools to estimate properties of each cell in the cell library (power, speed, yield, etc.) and to create the model of each cell in location S(x,y) with the assumed neighboring features.

19. A method for estimating properties (power, speed, yield, etc.) of each cell in a cell library and for creating a corresponding model of each cell, as a function of position (x,y) in the optical field, said method including the steps of:

A. labeling all gates of a layout of the cell in the cell library using the method of claim 3 and labeling the corresponding gates in the netlist according to category (cat), while assuming neighboring cells which have assumed features at an assumed distance;

B. varying L for each gate category according to an experimental design, as practiced by one of ordinary skill in the art, and inputting the modified netlist to standard software tools for each value of L to estimate properties of each cell in the cell library (power, speed, yield, etc.); and

C. generating a function (model) which represents the properties of each cell in the cell library (power, speed, yield, etc.) as a function of L for each category, using modeling methods known to those skilled in the art.

20. A method for estimating circuit properties (power, speed, yield, etc.), said method including the steps of:

A. creating models of all cells in a standard cell library as a function of position (x,y) in the optical field using the method of claim 18;

B. labeling all instances of standard cells in a circuit according to position (x,y) in the optical field; and

C. inputting the location-dependent models to standard software tools to estimate circuit properties (power, speed, yield, etc.).

21. A method for estimating circuit properties (power, speed, yield, etc.), said method including the steps of:

A. labeling all gates of a layout of each of the cells in the cell library by any or all of the following criteria to specify their category (cat): (i) orientation, (ii) neighborhood features within the same layer of the layout (for example, but not limited to the distance to nearest neighbors and/or more distant neighbors), and (iii) relative positions of neighboring structures within the same layer of the layout (for example, but not limited to east vs. west neighbors, north vs. south neighbors) and labeling the corresponding gates in the netlist according to category (cat), while assuming neighboring cells which have assumed features at an assumed distance;

B. creating models of all cells in the standard cell library as a function of gate length by varying L for each gate category according to an experimental design, as practiced by one of ordinary skill in the art, inputting the modified netlist to standard software tools to estimate properties of each cell in the cell library (power speed, yield, etc.) for each value of L, generating a function with represents the properties of each cell as a function of L for each gate category, using modeling methods known to those skilled in the art;

C. labeling all instances of standard cells in a circuit according to position (x,y) in the optical field;

D. determining L(x,y,cat) by creating CD(x,y,cat) by any method apparent to one of ordinary skill in the art or by any of the methods of claims 9, 10, 11, 12, 13, 14, 15, and 16, and by finding the relation between gate length, L, in the netlist, and CD, as would be easily determined by one skilled in the art; and

E. inputting the models from step A into standard software tools to estimate circuit properties (power, speed, yield, etc.), which lookup corresponding values of L(x,y,cat) during model evaluation.

22. A method for creating the layout of an integrated circuit (IC) chip, said method including the steps of:
    A. creating models of properties (area, speed, power, yield, etc.) for each of the blocks of a circuit as a function of position using one of the methods in claims 17, 18, 20, and 21; and
    B. inputting the models into a floor planning or other layout generation tool for use in the cost function, which guides layout generation.

23. A method for increasing the speed of an integrated circuit (IC) chip by modifying the layout, said method including the steps of:
    A. creating models of speed for each of the cells and blocks of a circuit as a function of position using one of the methods in claims 17, 18, 20, and 21;
    B. inputting the models to standard software tools to determine the critical paths of the circuit; and
    C. laying out the circuit so that cells and blocks most strongly influencing the speed of the circuit are placed in locations with smaller CD, where speed is measured by inputting the models of each of the cells into a standard CAD tool for timing estimation.

24. A method for reducing the power dissipation of an integrated circuit (IC) chip by modifying the layout, said method including the steps of:
    A. creating models of power dissipation for each of the cells and blocks of a circuit as a function of position using one of the methods in claims 17, 18, 20, and 21;
    B. inputting the models to standard software tools to determine the power dissipation of the circuit; and
    C. laying out the circuit so that cells and blocks most strongly influencing the power dissipation of the circuit are placed in locations with larger CD, where power

dissipation is measured by inputting the models of each of the cells into a standard CAD tool for power estimation.

25. A method for increasing the yield of an integrated circuit (IC) chip by modifying the layout, said method including the steps of:
    A. creating models of yield for each of the cells and blocks of a circuit as a function of position using one of the methods in claims 17, 18, 20, and 21; and
    B. laying out the circuit so that cells and blocks with lowest yield are placed in locations with larger CD.